CLAIMS

What is claim is:

1. A substrate for electrically interconnecting a semiconductor chip mounted thereon to an external device, the substrate comprising:

a ground plane electrically interconnected to a ground power of the semiconductor chip;

an insulating layer attached to the ground plane; and

a pattern layer attached to the insulating layer, the pattern layer comprising a signal pattern electrically interconnected to the semiconductor chip, and further comprising a ground pattern electrically interconnected to the ground plane,

wherein the ground pattern comprises a bonding land, the bonding land comprising a first via hole configured to electrically interconnect the ground pattern to the ground plane.

2. The substrate according to claim 1, wherein the first via holes comprises a blind via.

3. The substrate according to claim 1, further comprising a bonding wire electrically coupling the semiconductor chip to the bonding land.

4. The substrate according to claim 3, wherein the bonding wire is bonded to the first via hole.

5. The substrate according to claim 1, wherein the first via hole is filled with metal.

6. The substrate according to claim 1, wherein the first via hole has an inner surface plated with metal.

7. The substrate according to claim 1, wherein the signal pattern and the ground pattern comprise solder ball lands to which solder balls are attached.

8. The substrate according to claim 1, wherein the ground pattern further comprises a second via hole that is electrically interconnected to the ground plane.

9. The substrate according to claim 1, wherein the ground plane further comprises a first and a second ground plane separated by a centrally disposed opening.

10. The substrate according to claim 1, wherein the insulating layer is a polyimide tape and wherein the pattern layer and the ground plane each comprise copper.

11. The substrate according to claim 1, wherein the substrate is formed by forming the insulating layer on the ground plane, forming the first via hole within the insulating layer, and forming the pattern layer on the insulating layer.

12. The substrate according to claim 1, wherein the substrate is formed by sequentially stacking the ground plane, the insulating layer, and the pattern layer, and forming the first via hole therein.

13. The substrate according to claim 1, wherein the substrate is adapted for use in wafer level packages.

14. A semiconductor chip package comprising:

a semiconductor chip; and

a substrate configured to electrically interconnect the semiconductor chip mounted thereon with an external device, the substrate comprising:

a ground plane electrically interconnected to a ground power of the semiconductor chip;

an insulating layer attached to the ground plane; and

a pattern layer attached to the insulating layer, wherein the pattern layer comprises a signal pattern configured to communicate electrical signals with the semiconductor chip and a ground pattern electrically interconnected to the ground plane,

wherein the ground pattern comprises a bonding land to provide an electrical connection to the semiconductor chip, the bonding land comprising a first via hole configured to electrically interconnect the ground patterns to the ground plane.

15. A semiconductor chip package according to claim 14, further comprising a bonding wire bonded to the first via hole.

16. A semiconductor chip package according to claim 14, wherein the first via hole is filled with metal.

17. A semiconductor chip package according to claim 14, wherein the first via hole has an inner surface plated with metal.

18. A semiconductor chip package according to claim 14, wherein the signal pattern and the ground pattern comprise solder ball lands to which solder balls are attached.

19. A semiconductor chip package according to claim 14, wherein the ground pattern further comprises a second via hole electrically connected to the ground plane.

20. A semiconductor chip package according to claim 14, wherein the ground plane includes a first and a second ground plane separated by a centrally disposed opening.

21. A semiconductor chip package according to claim 14, wherein an exposed surface of the semiconductor is covered by an encapsulant.

22. A semiconductor chip package according to claim 14, wherein the semiconductor chip is attached to the substrate by an elastic adhesive.

23. A method of forming a semiconductor substrate configured to provide electrical connection between a semiconductor chip and an external device, the method comprising:

forming a ground plane on an insulating layer;

forming a via hole within the insulating layer; and

forming a pattern layer on the insulating layer, the pattern layer comprising a signal pattern and a ground pattern,

wherein the ground pattern comprises a bonding land for providing electrical connection to the semiconductor chip, the bonding land overlying the via hole for electrically coupling the ground pattern to the ground plane.

24. A method according to claim 23, wherein the ground plane and the pattern layer are formed on opposite sides of the insulating layer before forming the via hole.

25. A method according to claim 24, wherein the ground plane is formed on the insulating layer and the via hole is formed through the first insulating layer before the pattern layer is formed on the insulating layer.

26. A method according to claim 25, further comprising reducing a length of a return current path in the substrate by providing the via hole in close proximity with the signal pattern.

27. A method according to claim 26, wherein forming the ground plane comprises forming a first and second ground plane separated by a centrally disposed opening.